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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/574,866	05/19/2000	James M. Rehg	200308344-1	1569

7590 09/29/2004

IP Administration, Legal Department, MS35
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EXAMINER	
VO, LILIAN	
ART UNIT	**PAPER NUMBER**
2127	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/574,866	REHG ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09222004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 54 are pending.

Claim Objections

2. **Claim 51** is objected to because the examiner believes it should depend on claim 50 instead of claim 18.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 12, 15, 18 – 29, 32, 35 - 46, 49, 52 and 53 - 54 are rejected under 35 U.S.C. 103(a) as being unpatentable by Jevtic et al. (US 6,519,498, hereinafter Jevtic) in view of Babaian et al. (US Pat. Application Publication 2001/0042189, hereinafter Babaian).

5. Regarding **claims 1, 18, 35 and 53**, Jevtic teaches a scheduling method comprising steps of:

based on scheduling states, defining a set of static schedules for an application (abstract, fig. 3, col. 4, line 40 – col. 5, line 9, lines 32 – 53, col. 6, lines 31 – 61);

during run time, learning a cost of a set of static schedules based on performance of the application (abstract, fig. 3, col. 4, line 40 – col. 5, line 9, lines 32 – 53, col. 6, lines 31 – 61, col. 11, lines 3 – 13, col. 2, line 63 – col. 3, line 13); and

designating a static schedule with a lowest cost as an optimal schedule for a scheduling state (abstract, fig. 3, col. 4, line 40 – col. 5, line 9, lines 32 – 53, col. 6, lines 31 – 61, col. 11, lines 3 - 13, col. 2, line 63 – col. 3, line 13).

Jevtic however did not clearly disclose that each static schedule including an assignment of tasks to processors. Nevertheless, Babaian discloses static schedule including performs scheduling/assignment instructions/tasks to processors (page 1, paragraph 11, 12, page 2, paragraph 24, page 8, paragraph 86). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made to incorporate to Jevtic an explicit parallelism architecture processors and operation method of this system to help ensure a high level use of instruction level parallelism (page 2, paragraph 19).

6. Regarding **claim 2**, Jevtic teaches a scheduling method as claimed in claim 1 wherein the cost of a set of static schedules is learned each time there is a change in scheduling state (fig. 3 and col. 21, lines 46 – 50).

7. Regarding **claim 3**, Jevtic teaches a scheduling method as claimed in claim 1 wherein the cost of a set of static schedules is learned continuously during run time (fig. 3 and col. 21, lines 16 - 17).

8. Regarding **claim 4**, Jevtic teaches a scheduling method as claimed in claim 1 further comprising:

storing a set of all possible schedules associated with each schedule state (fig. 3); and

upon a change of state, selecting the optimal schedule associated with the schedule state (fig. 3).

9. Regarding **claim 7**, Jevtic teaches a scheduling method as claimed in claim 6 wherein the schedule is randomly selected dependent on utility of exploration associated with the schedule (abstract).

10. Regarding **claim 8**, Jevtic teaches a scheduling method as claimed in claim 1 wherein the cost of a schedule is computed and stored after the schedule is executed (fig. 3).

11. Regarding **claim 9**, Jevtic teaches a scheduling method as claimed in claim 1 further comprising:

maintaining a task execution cost for each task in the application for each schedule state (fig. 3).

12. Regarding **claims 11 and 12**, Jevtic teaches a method as claimed in claim 10 wherein the cost of a task/schedule is updated using stored task execution costs with recent schedule execution costs having more importance (fig. 3, col. 6, lines 10 – 61).

13. Regarding **claim 15**, Jevtic teaches a scheduling method as claimed in claim 1 wherein the step of learning further comprises:

storing application input data received during an active period in the application (col. 6, lines 16 – 39); and

exploring optimal schedules while replaying stored input data during an idle period in the application (col. 6, lines 16 – 53, col. 12, lines 48 - 60).

14. Regarding **claim 52**, Jevtic teaches a computer system comprising:

a CPU connected to a memory system by a system bus (fig 2);

an I/O system, connected to the system bus by a bus interface (fig. 2); and

a scheduling system routine located in the memory system (fig. 2) which:

based on scheduling states, defining a set of static schedules for an application (abstract, fig. 3, col. 4, line 40 – col. 5, line 9, lines 32 – 53, col. 6, lines 31 – 61);

during run time, learning a cost of a set of static schedules based on performance of the application (abstract, fig. 3, col. 4, line 40 – col. 5, line 9, lines 32 – 53, col. 6, lines 31 – 61, col. 11, lines 3 – 13, col. 2, line 63 – col. 3, line 13); and

designating a static schedule with a lowest cost as an optimal schedule for a scheduling state (abstract, fig. 3, col. 4, line 40 – col. 5, line 9, lines 32 – 53, col. 6, lines 31 – 61, col. 11, lines 3 - 13, col. 2, line 63 – col. 3, line 13).

Jevtic however did not clearly disclose that each static schedule including an assignment of tasks to processors. Nevertheless, Babaian discloses static schedule including performs scheduling/assignment instructions/tasks to processors (page 1, paragraph 11, 12, page 2, paragraph 24, page 8, paragraph 86). It would have been obvious for one of an ordinary skill in

the art, at the time the invention was made to incorporate to Jevtic an explicit parallelism architecture processors and operation method of this system to help ensure a high level use of instruction level parallelism (page 2, paragraph 19).

15. Regarding **claim 54**, Jevtic did not disclose the additional limitation as claimed. Nevertheless, Babaian discloses the performance of the application is based on time to complete one iteration of the application (page 3, paragraphs 41 - 43: the execution time for each wide instruction is equal one cycle). It would have been obvious for an ordinary skill in the art, at the time the invention was made, to incorporate this feature to Jevtic so that measurement can provide more accurate information for data analysis, thus enhance the all over system performance.

16. **Claims 5, 6, 10, 19 – 29, 32, 36 – 46 and 49** are rejected on the same ground as stated in claims 2 – 4, 7 – 9, 11, 12 and 15 above.

17. Claims 13, 14, 16, 17, 30, 31, 33, 34, 47, 48, 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jevtic (US 6,519,498) in view of Babaian (US Pat. Application Publication 2001/0042189) as applied to claims 1, 15, 18, 32, 35 and 49 above, in view of Dave (US 6,178,542).

18. Regarding **claim 13**, Jevtic and Babaian did not teach the additional limitation as claimed. Nevertheless, Dave teaches the step of:

predicting the cost of a schedule dependent on stored task execution costs (abstract, col. 12, lines 26 – 56, col. 15, lines 31 – 38, and figs 6 - 10).

It would have been obvious for one of an ordinary skill in the art, at the time the invention was made to incorporate Dave's teaching to Jevtic and Babaian's invention so that schedule estimation cost could be obtained to enhance system performance.

19. Regarding **claim 14**, Jevtic and Babaian did not teach the additional limitation as claimed. Nevertheless, Dave teaches a schedule is selected for further exploration dependent on the predicted schedule cost (abstract, col. 12, lines 26 – 56, col. 15, line 31 – col. 16, line 21, and figs 6 - 10). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made to incorporate Dave's teaching to Jevtic and Babaian's invention so that performance estimation cost could be obtained for more efficient scheduling.

20. Regarding **claim 16**, Jevtic and Babaian did not teach the additional limitation as claimed. Nevertheless, Dave teaches the step of concurrently executing a copy of an application with identical input data on a processor other than the processor on which the application is executing (col. 1, lines 34 – 41, col. 2, lines 29 – 33 and fig. 9: a system employs heterogeneous distributed architectures with several processors that run a large number of tasks concurrently). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made to incorporate Dave's teaching to Jevtic and Babaian's invention to provide the system with a capability of parallel processing on multiple processors.

21. Regarding **claim 17**, Jevtic teaches the additional limitation as claimed, wherein a change in the optimized schedules is immediately reflected to a schedule analyzer for use in the next schedule change of the application (abstract, fig. 3, col. 4, line 40 – col. 5, line 9, lines 32 – 53, col. 6, lines 31 – 61, col. 11, lines 3 - 13, col. 2, line 63 – col. 3, line 13 and fig. 3).

22. **Claims 30, 31, 33, 34, 47, 48, 50 and 51** are rejected on the same ground as stated in claims 13, 14, 16 and 17 above.

Response to Arguments

23. Applicants' arguments with respect to claims 1, 18, 35, 52 and 53 have been considered but are moot in view of the new ground(s) of rejection.

24. With respect to applicants' remark that Jevtic does not teach or suggest the limitation "based on scheduling states, defining a set of static schedules for the application" (page 14, last paragraph), the examiner disagrees. Jevtic clearly teaches this limitation in col. 4, line 40 – col. 5, line 9, in which a plurality of wafer processing schedules is being managed. Also in fig. 3 shows list of robots and scheduling algorithms that can be used to determine an optimal schedule (col. 6, lines 1 – 61).

Similarly, with respect to applicants' remark that Jevtic did not teach or suggest the limitation "during run-time, based on the scheduling state, learning a cost of a set of static schedules based on performance of the application" (page 15, 3rd paragraph), the examiner also disagrees. Jevtic clearly teaches this limitation in col. 4, line 40 – col. 5, line 9, in which during execution of the simulation associates with different schedule algorithms, the cost of each

schedule based on performance is learned and used for comparing to determine an optimal schedule (see also fig 3 and col. 6, lines 1 – 61).

25. In response to applicants' argument that dependents claims are non-obvious over the cited prior art (page 15, last paragraph – page 16, 1st paragraph), the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

26. Applicants' arguments (page 16, 2nd paragraph) fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2127

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SUPERVISORY PATENT EXAMINER
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lv
September 23, 2004